Speed Comparison Of 32x32 Multiplier using Vedic Mathematic Techniques

Hema S., Geethapriya S., Vijayalakshmi G.

Abstract— Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers . So the Implementation of Vedic Mathematic techniques and their application to the complex multiplier provide substantial reduction in propagation delay ,execution time in comparison with the existing methods. This paper proposed the design of high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. The techniques described in this paper are Nikhilam Sutra, Urdhva Tiryakbhyam and Karatsuba-ofman and the performance analysis of these techniques is obtained. Modelsim tool is used for simulation and the results obtained are compared on the basis of time delay of multiplication.

Index Terms— vedic mathematics, urdhva triyakbhyam sutra, karatsuba - ofman algorithm

I. INTRODUCTION

Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application . In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor.

In the past Due to the growth of computer and signal processing applications the demand for high speed processing has been increased. In order to achieve the desired performance in many real-time signal and image processing applications higher throughput arithmetic operations are important. Multiplication is one of the key arithmetic operations in such applications. Speed of multiplication operation is of great importance in DSP. The multiplier is a large block of computing system .The amount of circuitry involved is directly proportional to the square of its resolution.

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From delay perspective latency and throughput are the two major concerns in DSP applications for multiplication algorithm. Latency is the real delay of computing a function. Throughput is the measure of how many multiplications can be performed in a given period of time. Multiplier based on Vedic Mathematics is one of the fast multiplier as compared to other methodologies used for multiplication such as Array multiplier, Wallace tree and Booth multiplier. This paper describes the different techniques used in Ancient Vedic Mathematics for multiplication and also compares them.

II. VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful [2, 3].

The word "Vedic" is derived from the word **"Veda"** which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.

7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or noncompletion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. Shesanyankena Charamena – The remainders by the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing [1,4].

The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial-parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

III. DESIGN OF VEDIC MULTIPLIER

A.Urdhva – Triyagbhyam(Vertically and Crosswise)

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions.

An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Fig. 1. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

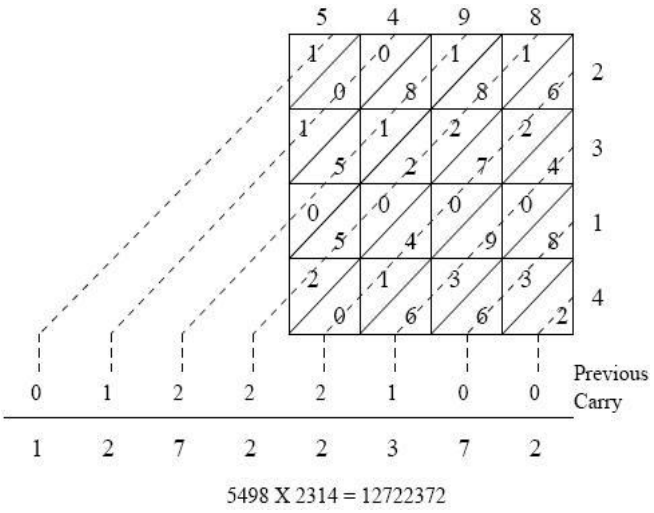

Fig 1: Alternative way of multiplication by Urdhva tiryakbhyam Sutra.

The design starts first with Multiplier design, that is 2x2 bit multiplier as shown in figure 2. Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, which is to add and shift the partial products.

Another way of multiplication of two numbers using this technique is as shown below in Fig. 2.

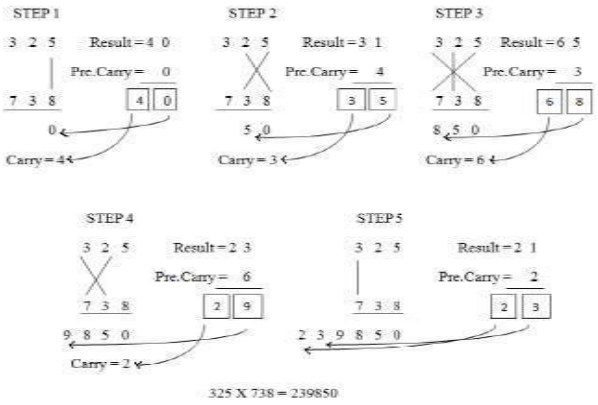

Fig. 2 Alternative method of Multiplication of two large integers

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.2.2. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero .

B. Nikhilam Sutra

Nikhilam Sutra literally

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means “all from 9 and last from 10”. Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. It finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, hence larger the original number, lesser the complexity of the multiplication. We first illustrate this Sutra by considering the multiplication of two decimal numbers (96 × 93) where the chosen base is 100 which is nearest to and greater than both these two

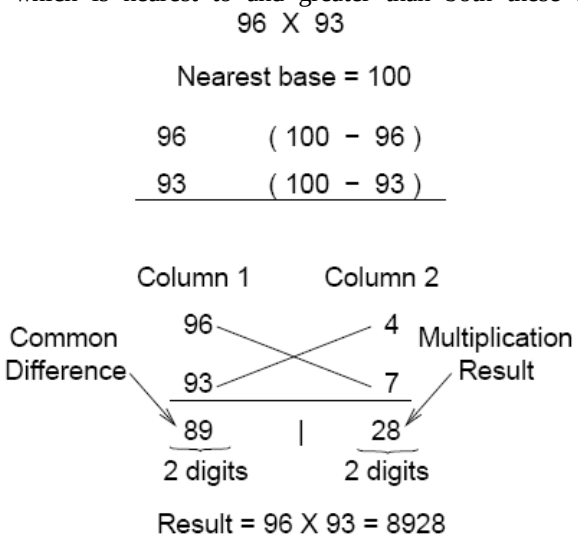

Fig 3. Line diagram for multiplication of two 4-bit numbers.

As shown in Fig. 3, we write the multiplier and the multiplicand in two rows followed by the differences of each of them from the chosen base, i.e., their compliments. We can now write two columns of numbers, one consisting of the numbers to be multiplied (Column 1) and the other consisting of their compliments (Column 2). The product also consists of two parts which are demarcated by a vertical line for the purpose of illustration. The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (7×4 = 28). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 96 - 7 = 89 or 93 - 4 = 89. The final result is obtained by concatenating RHS and LHS (Answer = 8928).

Architecture of Vedic Multiplier Using Nikhilam Sutra:

Broadly this architecture is divided into three parts.

(i) Radix Selection Unit

(ii) Exponent Determinant

(iii) Multiplier.

Hardware implementation of this multiplier is shown in Fig. 1 [4]. The architecture can be decomposed into three main subsections: (i) Radix Selection Unit (RSU) (ii) Exponent Determinant (ED) and (iii) Multiplier. The RSU is required to select the proper radices corresponding to the input numbers.

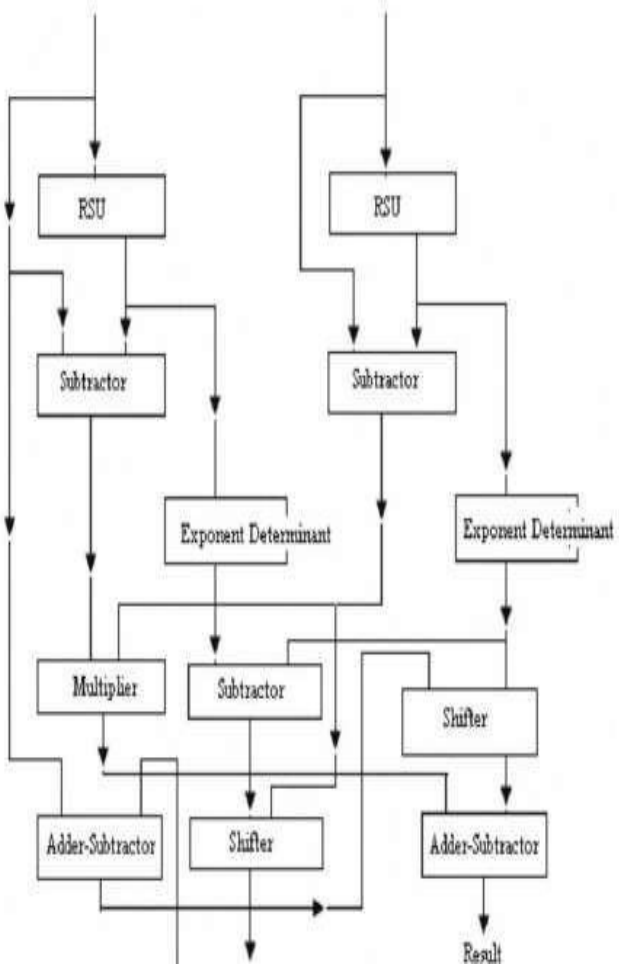

Fig 4. Multiplier architecture Design

C. Karatsuba-Ofman

Karatsuba-Ofman algorithm is considered as one of the fastest ways to multiply long integers. It is based on the divide and conquers strategy [3]. A multiplication of 2n digit integer is reduced to two n digit multiplications, one (n+1) digit multiplication, two n digit subtractions, two left shift operations, two n digit additions and two 2n digit additions.

Let A and B are the binary representation of two long integers. They can be written as follows:

$$A = \sum_{i=0}^{k-i} a_i 2^i$$

$$B = \sum_{i=0}^{k-1} b_i 2^i$$

We wish to compute the product A&B .Using the divide and conquer strategy,the operands A&B can be decomposed into equal size parts A_H and A_l , B_H and B_l , where subscripts H and L represent high and low order bits of A and B respectively. Let k= 2n. If k is odd, it can be right padded with a zero.

$$A = 2^n \sum_{i=0}^{n-1} a_{i+n} 2^i \quad \sum_{i=0}^{n-1} a_i 2^i \quad A_H 2^n \quad A_L$$

$$B = 2^n \sum_{i=0}^{n-1} b_{i+n} 2^i \quad \sum_{i=0}^{n-1} b_i 2^i \quad B_H 2^n \quad B_L$$

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The product AB can be computed as follows:

P = A * B

P = $(A_H 2^n + A_L)(B_H 2^n + B_L$

For Multiplier, first the basic blocks, that are the 2x2 bit multipliers have been made and then, using these blocks, 4x4 block has been made by adding the partial products using carry save adders and then using this 4x4 block, 8x8 bit block, 16x16 bit block and then finally 32 x 32 bit Multiplier as shown in figure 3 has been made.

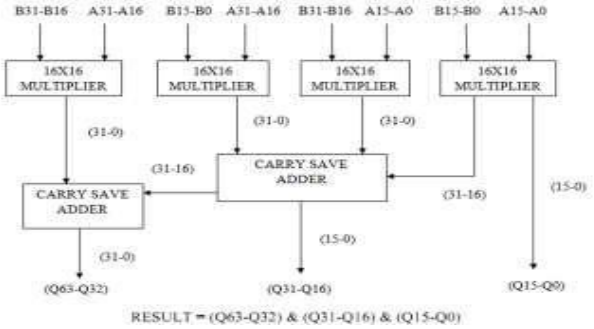
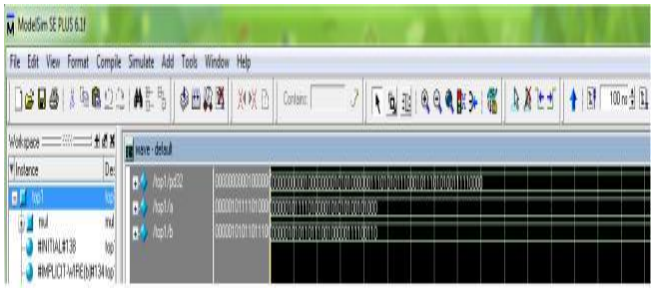


Fig 5: 32X32 Bits proposed Vedic Multiplier

IV. IMPLEMENTATION OF VEDIC MULTIPLIER

The proposed multiplications were implemented using two different coding techniques viz., conventional shift & add and Vedic technique for 4, 8, 16, and 32 bit multipliers. It is evident that there is a considerable increase in speed of the Vedic architecture. The simulation results for 32 bit multipliers are shown in the figures.

Simulation Results



Synthesis Results

Selected Device:	3s500efg320-5		
Number of Slices:	25 out of	4656	0%
Number of Slice Flip Flops:	36 out of	9312	0%
Number of 4 input LUTs:	48 out of	9312	0%
Number used as logic:	41		
Number used as Shift registers:	7		
Number of IOs:	9		
Number of bonded IOBs:	9 out of	232	3%
Number of GCLKs:	1 out of	24	4%

Output on LCD Screen = A0A0A09F5F5F5F60 (In hexa).

TABLE I Delay composition for different multipliers

Size	Algorithm	Delay in ns
8 Bit	Karatsuba Algorithm Optimized Vedic Multiplier	31.029 15.418
16 Bit	Karatsuba Algorithm Optimized Vedic Multiplier	46.811 22.604
32 Bit	Karatsuba Algorithm Optimized Vedic Multiplier	82.834 31.526

The worst case propagation delay in the Optimized Vedic multiplier case was found to be 31.526ns. To compare it with other implementations the design was synthesized on XILINX: SPARTAN: xc3s500e-5fg320[17]. Table 1 shows the synthesis result for various implementations. The result obtained from proposed Vedic multiplier is faster than Karatsuba Algorithm.

V. CONCLUSION

The designs of 32x32 bits Vedic multiplier have been implemented on Spartan XC3S500-5-FG320. The design is based on Vedic method of multiplication . The worst case propagation delay in the Optimized Vedic multiplier case is 31.526ns. It is therefore seen that the Vedic multipliers are much more faster than the conventional multipliers. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased. Urdhva tiryakbhyam, Nikhilam and Anurupye sutras are such algorithms which can reduce the delay, power and hardware requirements for multiplication of numbers. FPGA implementation of this multiplier shows that hardware realization of the Vedic mathematics algorithms is easily possible. The high speed multiplier algorithm exhibits improved efficiency in terms of speed.

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